REMARKS

As a preliminary matter, it is noted that newly cited USP No. 5,815,698 to Holmann et al., which the Examiner relied on in the pending § 103 rejection, was not listed in the PTO-892 form. Accordingly, it is respectfully requested that the Examiner list **USP No. 5,815,698 to Holmann et al.** in a PTO-892 form in the next Office Action to make the record clear that it was considered by the Examiner.

Claim 7 is objected to for a minor informality. It is respectfully submitted that the enclosed amendment obviates the alleged informality. Accordingly, it is respectfully requested that this objection be withdrawn.

Claim 7 stands rejected under 35 U.S.C. § 102 as being anticipated by Phillips et al. '743 ("Phillips"), and claims 7-8 stand rejected under 35 U.S.C. § 103 as being unpatentable over Eickemeyer et al. '460 in view of Holmann et al. '698 ("Holmann"). Claim 7 is independent. These rejections are respectfully traversed for the following reasons.

Claim 7 recites in pertinent part, "instruction parallelizing/executing means for executing the two instructions, which designate the first execution unit as a target, in parallel by allocating one of the two instructions to the second execution unit, wherein the parallelizing/executing means is configured to convert one of the two instructions to another equivalent instruction that designates the second execution unit." According to one exemplary embodiment of the present invention, it can be made possible to provide the capability of converting one of two instructions which designate the same execution unit, which would preclude parallel execution thereof, to

another equivalent instruction which designates a different execution unit so as to enable parallel execution of the two instructions. For example, in one exemplary embodiment of the present invention illustrated in Figures 21,23 of Applicants' drawings, of the following two instructions "asl 2, R0" (a second instruction slot of the No. 2 instruction) and "asl 2, R2" (a second instruction slot of the No. 3 instruction), the instruction "asl 2, R2" can be converted to "add R2, R2" (a first instruction slot of the No. 2 instruction) shown in Fig. 23 (*see* corresponding disclosure in Applicants' specification). See also Figures 25-27 of Applicants' drawings for another exemplary embodiment, in which a first instruction A (add R3, R2) and second instruction B (add R0, R0) designate the same execution unit. According to the present invention, the second instruction B can be converted to instruction E (asl 1, R0) so as to enable the first instruction A and converted second instruction E to be executed in parallel (during period t2 to t3; *see* Figure 27).

Turning to the cited prior art, the Examiner relies exclusively on Phillips and Holmann as allegedly disclosing the claimed instruction parallelizing/executing means. However, it is respectfully submitted that neither Phillips nor Holmann disclose or suggest "instruction parallelizing/executing means for executing the two instructions, ***which designate the first execution unit as a target***, in parallel ***by allocating one of the two instructions to the second execution unit***, wherein the parallelizing/executing means is ***configured to convert one of the two instructions to another equivalent instruction that designates the second execution unit***" (emphasis added).

Phillips discloses only conventional parallel processing using ALU1 and ALU2 as shown in Figure 2. Phillips is completely silent as to a conversion of one instruction to another equivalent instruction much less in the manner recited in claim 7. Rather, Phillips discloses the

combined use of a 3-1 ALU along with a standard 2-1 ALU to effect parallel execution where the 2-1 ALU executes the first of two issued instructions while the 3-1 ALU executes the second thereof. Phillips does not disclose that the first and second instructions originally designated the same ALU, and thereafter one of the two instructions is converted to an equivalent instruction which designates the other ALU (*see, e.g.,* col. 4, lines 1-6). Indeed, Phillips has no disclosed need or desire for such a configuration.

Similarly, the alleged "conversion" of Holmann is directed merely to rearranging the instructions in two columns and inserting a NOP in one column where the two instructions (SRA and SUB) can not be executed in parallel because of a register dependency therebetween (*see, e.g.,* col. 2, lines 43-59). As can be seen in Figures 3-4 of Holmann, none of the instructions are converted into an equivalent instruction. Rather, SUB r4, r4, r3 is simply moved to the first column so as to avoid parallel placement with SRA r3, r3, 1, while the NOP instruction is written into the slot left open by the SUB instruction. Accordingly, Holmann merely discloses a rearrangement and insertion of instructions rather than a conversion of one instruction designating a first execution unit into another equivalent instruction designating a second execution unit.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently (noting that "inherency may not be established by probabilities or possibilities", *Scaltech Inc. v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999)), in a single prior art reference, *Akzo N.V. v. U.S. Int'l Trade Commission*, 808 F.2d 1471 (Fed. Cir. 1986), based on the forgoing, it is submitted that Eickemeyer does not anticipate claim 7, nor any claim dependent thereon. The Examiner is directed to MPEP § 2143.03 under the section

entitled "All Claim Limitations Must Be Taught or Suggested", which sets forth the applicable standard for establishing obviousness under § 103:

> To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (citing *In re Royka*, 180 USPQ 580 (CCPA 1974)).

In the instant case, the pending rejection does not "establish *prima facie* obviousness of [the] claimed invention" as recited in claims 7-8 because the proposed combination fails the "all the claim limitations" standard required under § 103.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 7 is patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejection under 35 U.S.C. § 102 be withdrawn.

CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's

amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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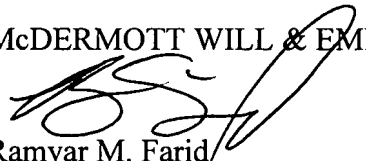

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